LOW VOLTAGE SENSING CIRCUIT FOR NON-VOLATILE MEMORY DEVICE

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ABSTRACT

Low voltage sensing circuits for non-volatile memory (NVM) devices including a comparator (operational amplifier) having input terminals connected to the gate terminals of first and second PMOS transistors. The PMOS transistors are coupled between a system voltage source and respective bit lines carrying cell and reference currents from a selected NVM cell and a reference NVM cell, respectively. To facilitate low system voltages, voltage supply or source-follower circuits are connected between the gate and drain terminals of each PMOS transistor such that the bit line voltages are increased without increasing the voltage signals applied to the input terminals of the comparator, and without the use of charge pumps.